MP023

Primary Side CC/CV Flyback Controller with High Voltage Current Source and Programmable Cable Compensation

The Future of Analog IC Technology

DESCRIPTION

The MP023 is an offline, primary-side controller that provides accurate, constant voltage and constant current regulation without the need of an optocoupler or secondary feedback circuit. It uses an integrated 700V current source to achieve quick start-up.

The MP023's variable off-time control allows its flyback converter to operate in discontinuous conduction mode (DCM). The MP023's current limit and maximum secondary duty cycle are programmable, making the output current easily set. The FB voltage sensing point is also programmable and is able to set different switching frequencies.

The internal high-voltage start-up current source and power-saving technologies limit the no-load power consumption to less than 30mW. Full protection features include VCC under-voltage lockout (UVLO), overload protection (OLP), over-temperature protection (OTP), open loop protection (OCkP), and over-voltage protection (OVP).

The MP023's variable switching frequency method provides a natural spectrum for shaping a smooth EMI signature, which is suitable for offline, low-power battery chargers and adapters.

The MP023 requires a minimal number of readily available, standard, external components and is available in a SOIC8-7A package.

FEATURES

- Primary-Side Control without Optocoupler or Secondary Feedback Circuit
- Precise Constant Current and Constant Voltage Control (CC/CV)
- Variable Off-Time Peak Current Control
- 700V High-Voltage Current Source
- 20mW No-Load Power Consumption
- Programmable Cable Compensation
- Programmable Current Limit and Maximum Secondary Duty Cycle
- Programmable FB Voltage Sensing Point
- Multiple Protection Features: OVP, OCkP, OLP, OTP, VCC UVLO
- Low Cost and Simple External Circuit
- Available in a SOIC8-7A Package

APPLICATIONS

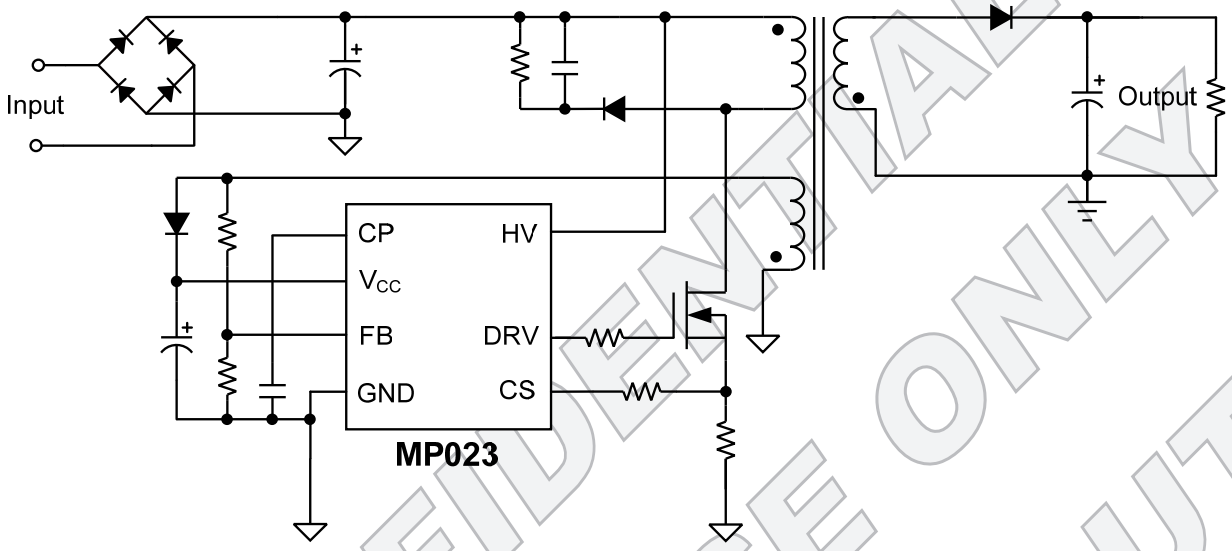
- Appliance Power Supplies
- Adapters for Handheld Electronics
- Standby and Auxiliary Power Supplies

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TYPICAL APPLICATION



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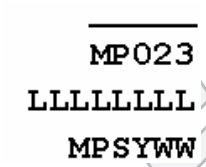
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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP023GS	SOIC8-7A	See Below

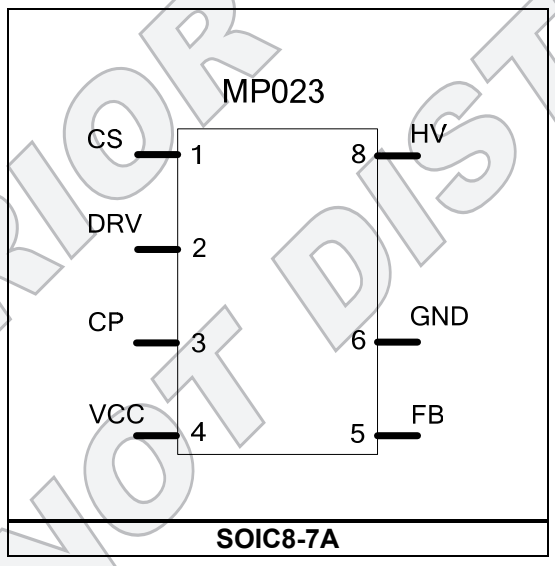
* For Tape & Reel, add suffix –Z (e.g. MP023GS–Z)

TOP MARKING



MP023: first five digits of the part number;
LLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

PACKAGE REFERENCE



SOIC8-7A

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ABSOLUTE MAXIMUM RATINGS (1)

HV to GND.....-0.3V to 700V
VCC to GND……..…….-0.3V to 28V
DRV to GND.....-0.3V to 15V
CP, CS to GND……....-0.3V to 7V
FB……...-0.7V to 7V
Maximum power dissipation (2)…..……1.3W
Junction temperature……..……..150°C
Lead temperature……260°C
Storage temperature…….-60°C to +150°C
ESD capability human body mode…..……2.0kV
ESD capability machine mode…….……200V

Recommended Operating Conditions (3)

Junction temp. (T_J)……...-40°C to +125°C
Operating VCC range……..……10V to 25V

Thermal Resistance (4)	θ_{JA}	θ_{JC}
SOIC8-7A……96	..... 45...	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 15V, T_J = -40℃~125℃, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage Management (VCC Pin)						
VCC ON threshold	V_{CCH}		18.8	19.4	20.0	V
VCC OFF threshold	V_{CCL}		8.2	8.7	9.2	V
Operating current	I_{OP}	f_{S-min}, C_L=1nF		245	300	μA
		fs = 40kHz, C_L=1nF		1	1.3	mA
High Voltage Current Source (HV Pin)						
Break-down voltage	V_{BRDSS}		700			V
Supply current from HV pin		V_{CC}=18V, V_{HV}=80V, T_J=25℃	1.8	2.1	2.5	mA
Leakage current from HV pin	I_{leak}	V_{DS}=400V_{dc}, T_J=25℃			10	μA
Driving (Drv Pin)						
Driver voltage high level	V_{High}	C_L=1nF V_{CC}=9.5V	7.2	7.8		V
Driver voltage clamp level	V_{Clamp}	C_L=1nF, V_{CC}=24V	12	13.4	15	V
Driver voltage low level	V_{Low}	C_L=1nF, V_{CC}=24V			50	mV
Driver voltage rise time	t_R	C_L=1nF		30		ns
Driver voltage fall time	t_F	C_L=1nF		40		ns
Maximum ON time	t_{ONmax}	V_{CS}=0V	24	38	51	us
Minimum switching frequency	f_{S-min}			72	105	Hz
Current Sense (CS Pin)						
Current limit	$V_{Limit-Max}$	f_S >= f_{S-H}	464	480	496	mV
	$V_{Limit-Min}$	f_S <= f_{S-L}	220	245	270	mV
fs to start the current fold back	f_{S-H}		30	40	48	kHz
fs to end the current fold back	f_{S-L}			20		kHz
Propagation delay to Drv	t_{PD}			60	95	ns
Leading edge blanking	t_{LEB}		180	280	380	ns
Feedback input (FB Pin)						
FB pin input current	I_{FB}	V_{FB} = 4V, V_{CP}=2V		12.5		μA
		V_{FB} = 4V, V_{CP}=1.5V		9.3		μA
		V_{FB} = 4V, V_{CP}=0.8V		4.8		μA
		V_{FB} = 4V, V_{CP}=0.2V		1.2		μA
FB reference voltage	V_{FB}		3.90	3.96	4.02	V
OLP threshold at sampled FB(5)	V_{FBolp}			1.4		V
OLP counter(1)				768		
FB sampling duration	t_{FB_SD}		180	250	330	ns
FB maximum sampling time	$t_{FBS-Max}$	R_{CS}=0Ω, V_{Limit}=0.5V	2.50	3.45	4.70	μs
		R_{CS}=1kΩ, V_{Limit}=0.5V	1.70	2.58	3.50	
		R_{CS}=2kΩ, V_{Limit}=0.5V	3.60	5.20	7.00	
		R_{CS}=4kΩ, V_{Limit}=0.5V	5.00	7.00	9.20	

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ELECTRICAL CHARACTERISTICS

V_{CC} = 15V, T_J = -40℃~125℃, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
FB minimum sampling time	$t_{FBS-Min}$	R_{CS}=0Ω, V_{Limit}=0.25V	1.00	1.70	2.50	µs
		R_{CS}=1kΩ, V_{Limit}=0.25V	0.68	1.28	1.88	
		R_{CS}=2kΩ, V_{Limit}=0.25V	1.70	2.57	3.50	
		R_{CS}=4kΩ, V_{Limit}=0.25V	2.50	3.42	4.70	
ZCD threshold	V_{DCM}		55	100	145	mV
FB open-circuit threshold	V_{FBopen}		-0.18	-0.105	-0.045	V
OVP threshold at FB	V_{FBovp}		5.7	6.0	6.3	V
FB OVP blanking time	t_{OVP-B}		0.92	1.23	1.53	µs
Output Cable Compensation (CP Pin)						
Supply voltage on CP	V_{CP-Max}			4		V
Thermal Shutdown						
Thermal shutdown threshold(5)				140		°C
Thermal shutdown hysteresis(5)				40		°C

Notes:
(5) The parameters are guaranteed by characterization.

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PIN FUNCTIONS

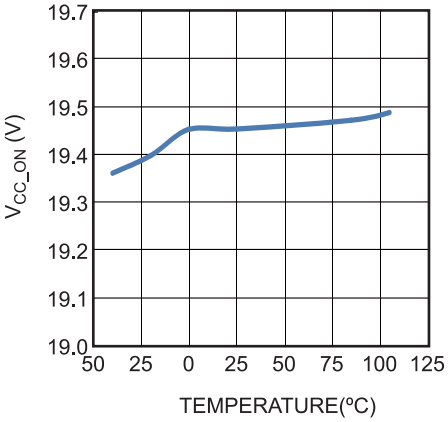
SOIC8-7A Pin #	Name	Description
1	CS	**Current sense.** CS connects to the current sense resistor to detect the MOSFET current for peak current mode control in CV and CC modes. CS can also be used to select a sampling time by different external resistor configurations. Connect CS to current sensing resistor directly, if default sampling time is selected. Please refer to EC table for additional details of sampling time selection.
2	DRV	**Driver.** DRV drives the external power MOSFET.
3	CP	**Output cable compensation.** Usually, a 1µF ceramic capacitor can be connected to CP as a low pass-filter. The compensation voltage can be adjusted by the divided resistor. CP can also be used to select the secondary duty limitation by different external resistor configurations. Short CP to GND, if default secondary duty is selected and cable compensation isn't required. Please refer to Table 1 for additional details.
4	VCC	**Supply voltage of the IC.** When VCC is lower than a certain level (V_{CCL}), the internal high-voltage current source is turned on to charge VCC. When VCC is charged to a certain level (V_{CCH}) by the internal high-voltage current source, the IC begins working. Connect a 0.1µF ceramic capacitor as close to VCC as possible to decouple the noise and the bulk capacitor.
5	FB	**Feedback.** Voltage on FB determines the operation mode (CV or CC mode).
6	GND	**Ground.**
8	HV	**Internal high-voltage current source.** HV draws current from the bus to charge up VCC for start-up.

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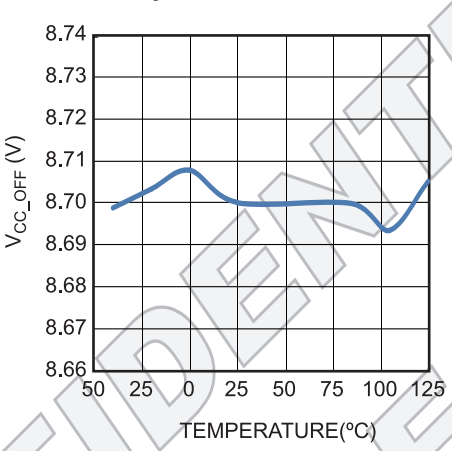
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TYPICAL CHARACTERISTICS

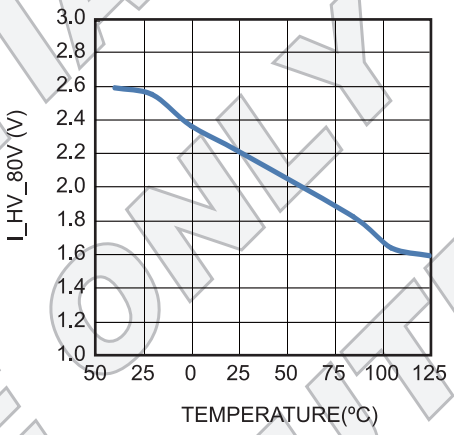
V_{CC_ON} vs. Temperature



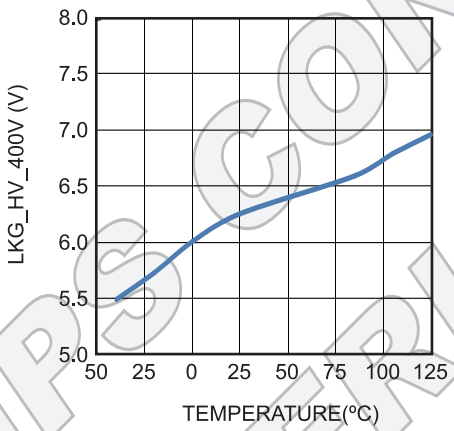
V_{CC_OFF} vs. Temperature



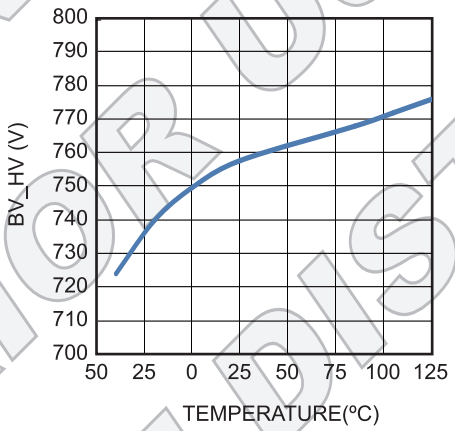
I_HV_80V vs. Temperature



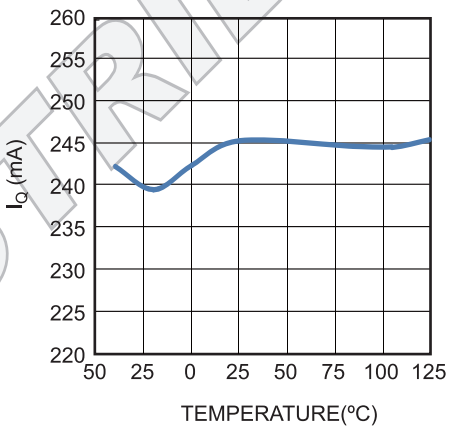
LKG_HV_400V vs. Temperature



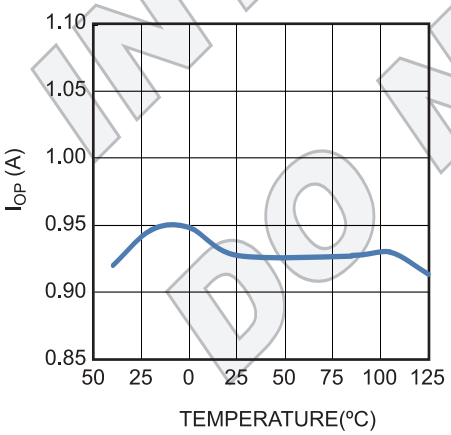
BV_HV vs. Temperature



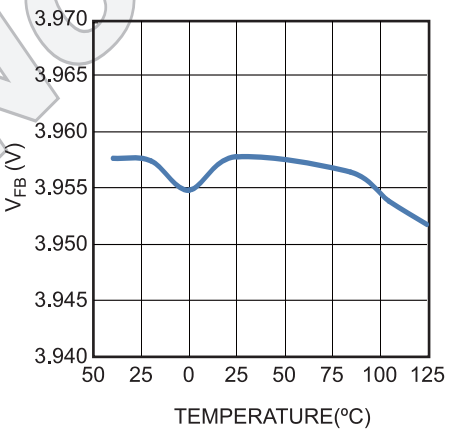
I_Q vs. Temperature



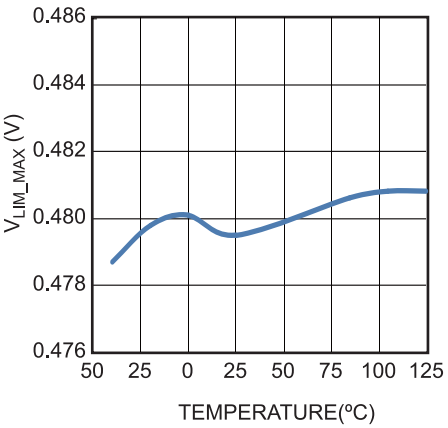
I_{OP} vs. Temperature



V_{FB} vs. Temperature



V_{LIM_MAX} vs. Temperature

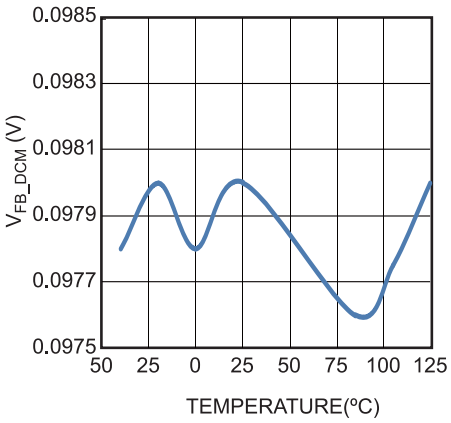


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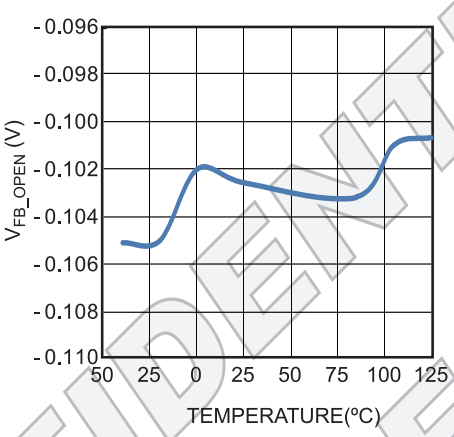
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TYPICAL CHARACTERISTICS *(continued)*

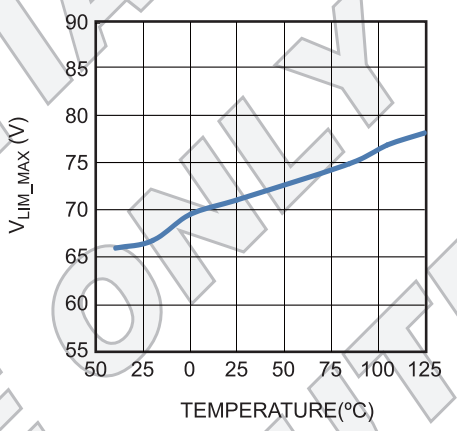
V_{FB_DCM} vs. Temperature



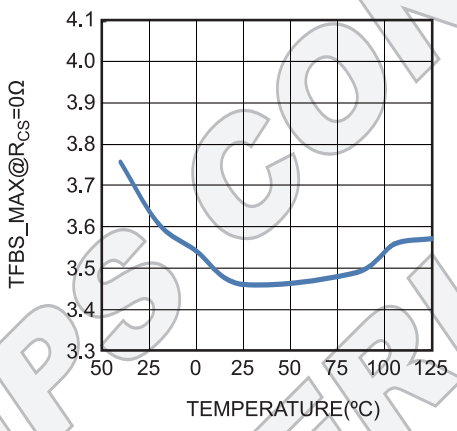
V_{FB_OPEN} vs. Temperature



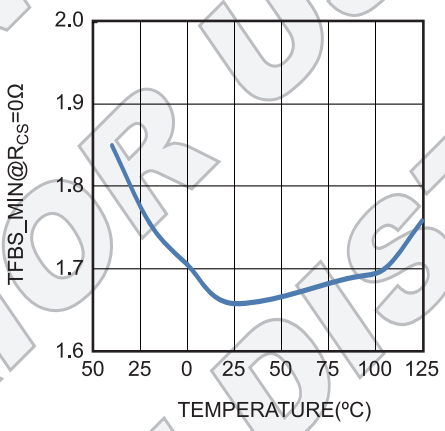
V_{LIM_MAX} vs. Temperature



TFBS_MAX@R_{CS}=0Ω vs. Temperature



TFBS_Min@R_{CS}=0Ω vs. Temperature



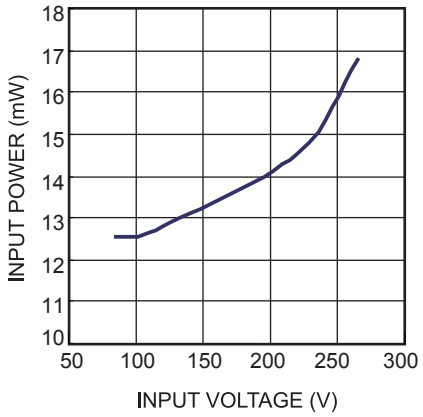
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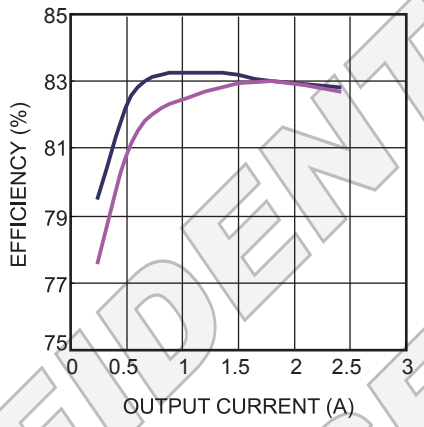
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 230V_{AC}, unless otherwise noted.

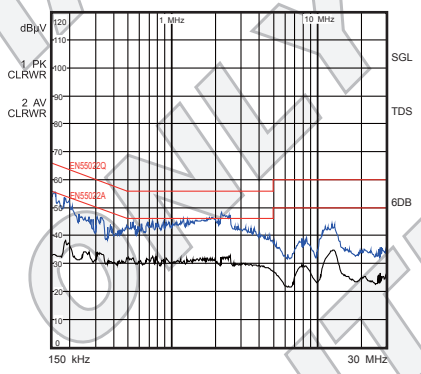
No Load Power Consumption



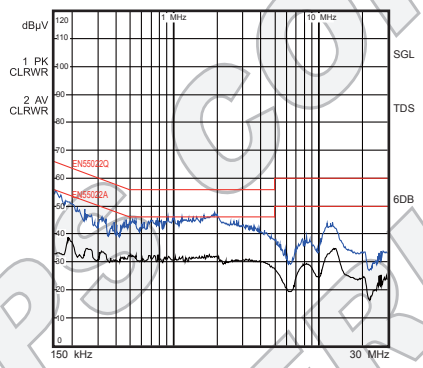
Efficiency vs. Load Current



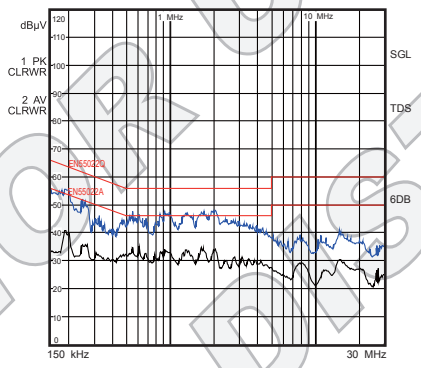
Conducted EMI
V_{IN}=115V_{AC}, L Line



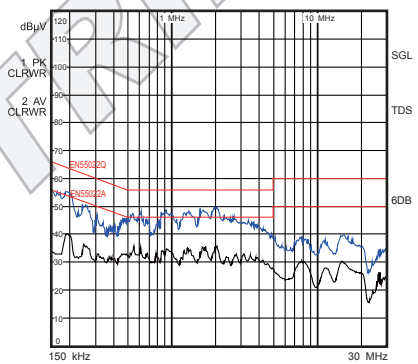
Conducted EMI
V_{IN}=115V_{AC}, N Line



Conducted EMI
V_{IN}=230V_{AC}, L Line



Conducted EMI
V_{IN}=230V_{AC}, N Line



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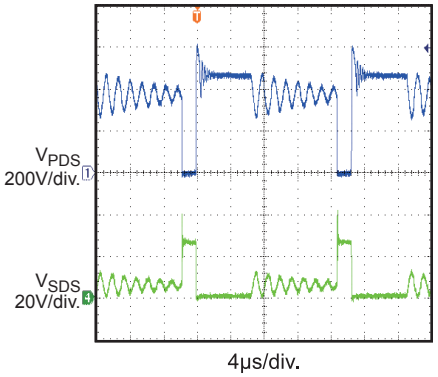
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 230V_{AC}, unless otherwise noted.

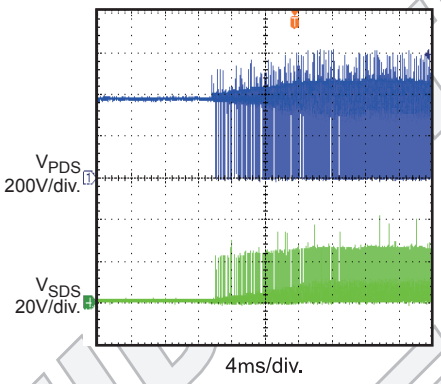
Steady State

V_{IN} = 265V_{AC}

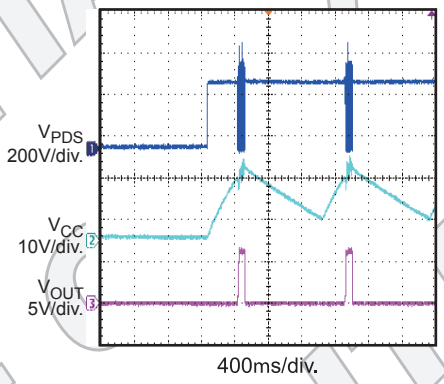


Power On

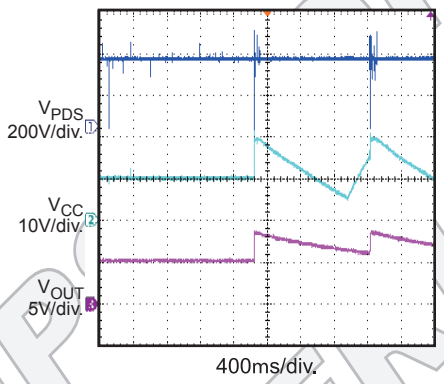
V_{IN} = 265V_{AC}



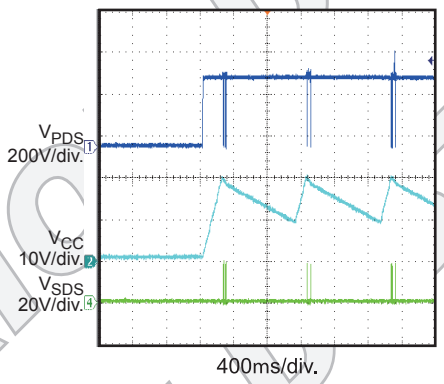
OVP Power On



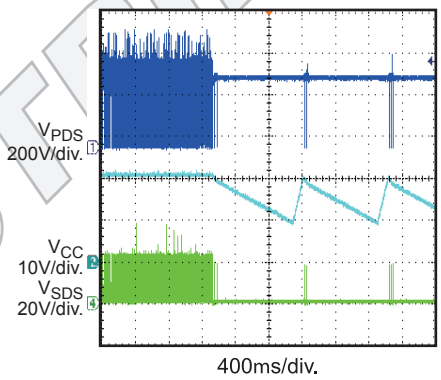
OVP Entry



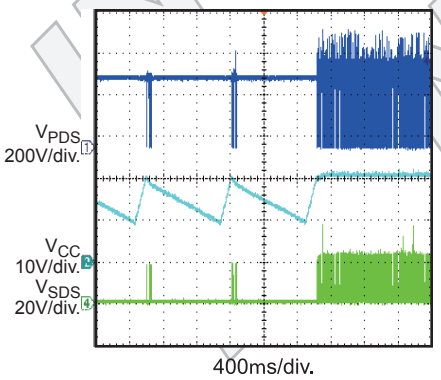
SCP Power On



SCP Entry



SCP Recovery



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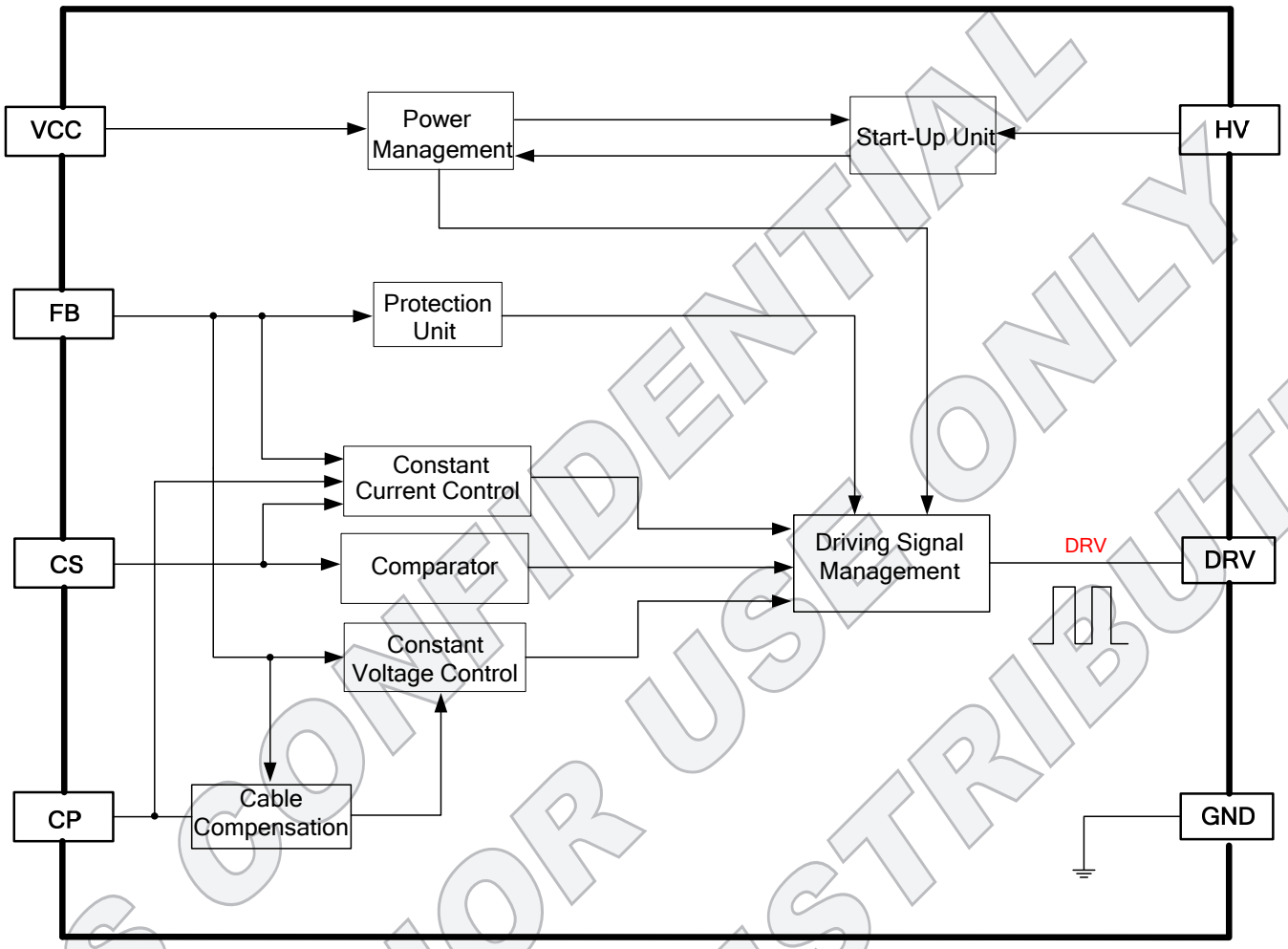


Figure 1: Functional Block Diagram

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OPERATION

The MP023 is a primary-side controller that provides accurate, constant voltage and constant current regulation without the need of an optocoupler or secondary feedback circuit. As shown in the Typical Application diagram, the circuit is designed to operate with a minimal number of external components.

Start-Up

The IC is self-supplied by the internal high-voltage current source, which is drawn from HV. Once the voltage on VCC reaches the VCC on threshold (V_{CCH}), the internal high-voltage current source turns off for better efficiency. Afterward, the auxiliary winding of the transformer takes over the power supply. When VCC falls below the VCC off threshold (V_{CCL}), the IC stops switching, and the internal high-voltage current source turns on again (see Figure 2).

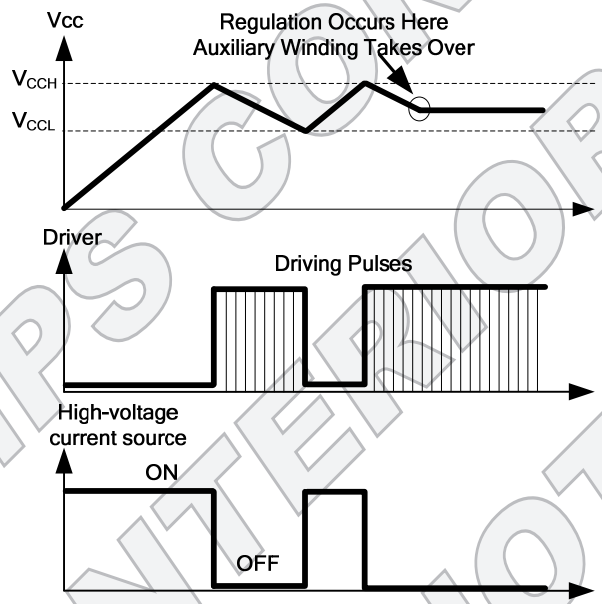


Figure 2: VCC UVLO

Peak Current Control on the Primary Side

The MP023 senses the primary current $I_P(t)$ through the current sense resistor (R_S), shown in Figure 3.

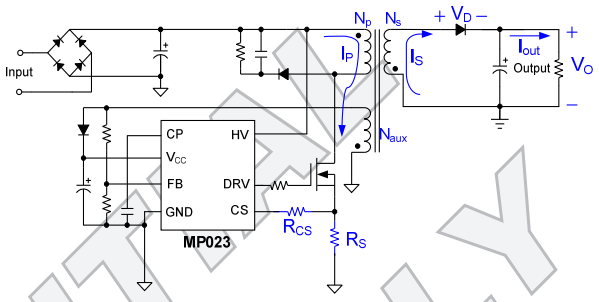


Figure 3: Simplified Flyback Converter

The current rises linearly at a rate shown in Equation (1):

$$\frac{dI_P(t)}{dt} = \frac{V_{in}}{L_m} \quad (1)$$

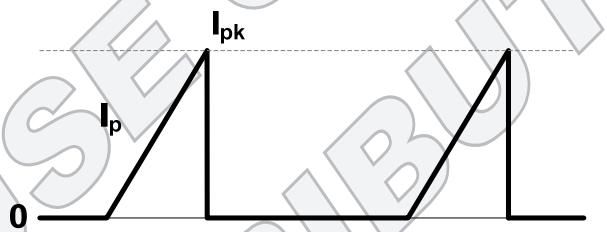


Figure 4: Primary Current Waveform

When the current $I_p(t)$ rises up to I_{pk} (see Figure 4), the primary switch turns off. The value of I_{pk} can be calculated with Equation (2):

$$I_{pk} = \frac{V_{CS}}{R_S} \quad (2)$$

The inductor (L_m) stores energy with each cycle. See Equation (3):

$$E = \frac{1}{2} L_m I_{pk}^2 \quad (3)$$

The power transferred from the input to the output can be calculated with Equation (4):

$$P = \frac{1}{2} L_m I_{pk}^2 f_s \quad (4)$$

Where f_S is the switching frequency.

In constant current (CC) operation, the reference for I_{pk} is fixed at $V_{Limit-Max}$. In constant voltage (CV) operation, I_{pk} is modulated by the switching frequency (see Figure 5).

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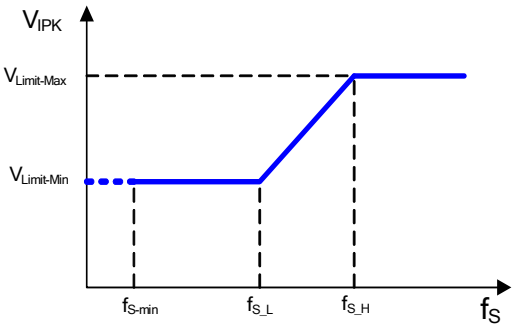


Figure 5: Peak Current Modulation

In the event that the external current sensing resistor is shorted, the maximum turn-on time is limited internally at t_{ONmax}. If this maximum limitation is reached, the IC enters protection mode.

Constant Voltage (CV) Operation

The MP023 detects the auxiliary winding voltage from FB and operates in constant voltage (CV) mode to regulate the output voltage.

The auxiliary voltage can be calculated with Equation (5):

$$V_{aux} = \frac{N_{aux}}{N_s}(V_O + V_D) \quad (5)$$

Where V_D is the forward drop voltage of the secondary diode.

During the conduction time of the secondary diode, the difference between the output voltage and the voltage on the secondary winding is not constant since V_D varies with the current flowing through the diode. To compensate for the voltage drop difference, the sampling time decreases gradually from $t_{FBS-Max}$ to $t_{FBS-Min}$ as the current limitation folds back from $V_{Limit-Max}$ to $V_{Limit-Min}$ (see Figure 6).

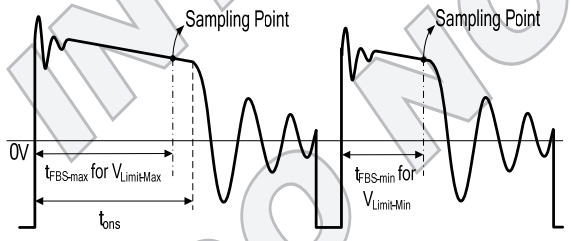


Figure 6: FB Voltage Sampling Point

The FB sampling time is also customizable with different resistor values connected to CS (see Figure 7). Please refer to EC table for details.

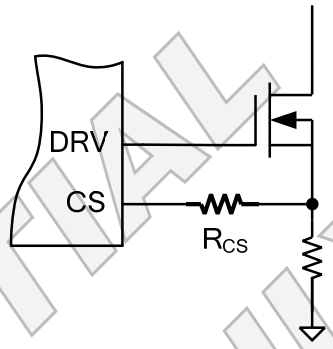


Figure 7: External Resistor for Sampling Time Customization

Choose a sampling time toward the end of the secondary diode conduction period to improve the accuracy of the CV regulation. The CV regulation loop then generates the switching frequency to regulate the output voltage based on the sampled voltage.

Constant Current (CC) Operation

Figure 8 shows the secondary current waveforms.

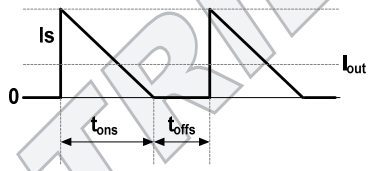


Figure 8: Secondary Current Waveform

In constant current (CC) operation, the CC loop control function remains at a fixed ratio between the secondary diode on time (t_{ons}) and the secondary diode off time (t_{offs}) by charging or discharging the internal capacitance. The fixed ratio limits the maximum duty of the secondary side diode on time, as shown in Equation (6):

$$\frac{t_{ons}}{t_{ons} + t_{offs}} = D_{S-Max} \quad (6)$$

For applications with varying output voltages, the D_{S-Max} can be customized with CP. If CP is connected with a capacitor directly or shorted to GND, the D_{S-Max} remains at a default value of 0.4. However, if CP is connected with a resistor (Figure 9), several choices are available based on the different resistances.

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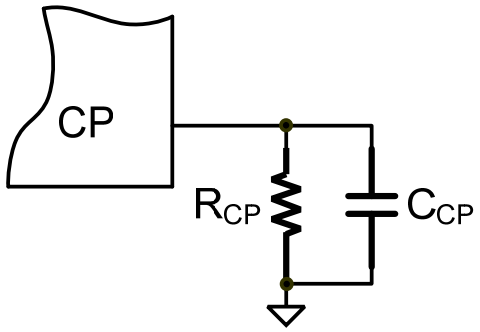


Figure 9: The External Configuration of CP

Table 1 shows all available values for D_{S-Max}. The entire customization process is completed before start-up and latched in a register, so it does not have any influence on normal operation.

Table 1: D_{S-Max} vs. CP Configuration

R_{CP}/C_{CP}	D_{S-Max}
0 Ω/NC*	0.4
10 kΩ/NC	0.3
20 kΩ/NC	0.35
40 kΩ/NC	0.5
NC/1μF	0.4

Notes:
* NC means no connection.

I_{pk} is also fixed in CC operation. The relationship between the output constant current and secondary peak current (I_{pks}) can be calculated with Equation (7):

$$I_{out} = \frac{1}{2} I_{pks} \frac{t_{ons}}{t_{ons} + t_{offs}} = \frac{1}{2} I_{pks} D_{S-Max} \quad (7)$$

When the secondary diode is turned on, the peak current on the secondary side is calculated with Equation (8):

$$I_{pks} = \frac{N_p}{N_S} I_{PK} \quad (8)$$

The output current is then calculated with Equation (9):

$$I_{out} = \frac{1}{2} \frac{N_p}{N_S} I_{PK} D_{S-Max} \quad (9)$$

To implement the OLP function in CC mode, the sampling on the FB voltage continues running with the sampling time fixed at $t_{FBS-Max}$.

Leading Edge Blanking

Turning the power switch on induces a spike on the sense resistor. The MP023 employs a leading edge blanking period (t_{LEB}) to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled, and the part cannot be turned off.

DCM Detection

The MP023 is designed to operate in discontinuous conduction mode (DCM) in both CV and CC modes. To avoid operating in continuous conduction mode (CCM), the MP023 implements a zero current detection (ZCD) function internally with a threshold of V_{DCM}. The IC does not start the next cycle until ZCD is detected.

During normal operation, the blanking time for ZCD is synchronized with the FB sampling time (i.e., ZCD always starts after the sampling phase is done). There is also a soft-start function on the ZCD blanking time to prevent ZCD from being triggered falsely when the output capacitor is not charged up. During the start-up period, the blanking time for ZCD shrinks gradually from t_{B_STP} (10μs) to the FB sampling time in 3 cycles.

OVP, OCkP, and OLP

The MP023 includes over-voltage protection (OVP), open-circuit protection (OCkP), and overload protection (OLP). If the voltage on FB exceeds V_{FBovp}, OVP is triggered. If V_{FBopen} cannot be monitored for each cycle, OCkP is triggered. If the sampled FB voltage is lower than V_{FBolp} for 128 consecutive cycles, OLP is triggered. When any of these protections are triggered, the MP023 shuts off immediately, enters hiccup mode, and resumes normal operation (t_{ons}) when the fault has been removed.

OLP is not enabled until the soft-start period of the ZCD blanking time is finished.

Over-Temperature Protection (OTP)

When the temperature of the IC exceeds 150°C, the over-temperature protection (OTP) is activated, and the IC enters auto-recovery mode. When the temperature falls below 120°C, the IC resumes operation.

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Output Cable Compensation

The MP023 has an internal output cable compensation (CP) circuit (see Figure 10). A switching signal (V_{CS_Lim}*D_{ons}) is generated internally and is synchronized with the switching frequency. The duty on-time of this signal is D_{ons}, and the amplitude of this signal is proportional to the current-limit threshold. This signal is output to CP through a 1MΩ resistor. A low pass filter can be implemented by placing an external capacitor on CP, and then a DC voltage (V_{CP}) proportional to the output current can be deducted on CP. Note that if cable compensation function is needed, D_{S-Max} is default as 0.4 and can't be programmable by connecting external CP resistor.

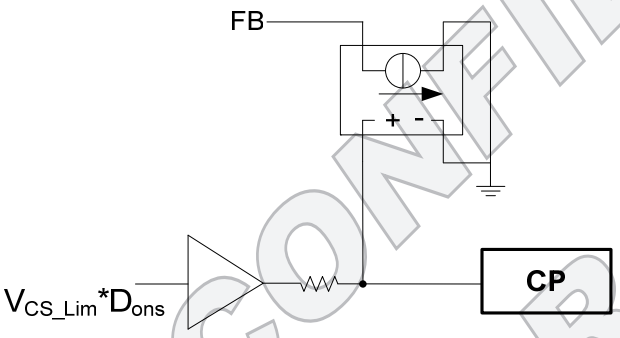


Figure 10: Output Cable Compensation

Table 2 shows some typical voltage levels on CP when a low pass filter is applied as described above.

Table 2: Typical CP Voltage Levels (C_{CP} = 1μF)

V_{Limit}	D_{ons}	V_{CP}
500mV	0.4	1.6V
500mV	0.35	1.4V
400mV	0.3	0.96V
250mV	0.1	0.2V

An internal current sink in FB is proportional to V_{CP}. The voltage drop on the upper resistor of the divider implements the output cable compensation function.

Since CP is also used for D_{S-Max} customization, the cable compensation function is only available when CP is connected to the capacitors directly. If there is a non-zero resistor connected to CP, all of the internal blocks related to the cable compensation function are disabled. During normal operation under this condition, CP is clamped to GND internally and there is no current flowing through FB.

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APPLICATION INFORMATION

Input Filter

The input filter helps to convert the AC input voltage to DC voltage. Figure 11 shows the input filter, and Figure 12 shows the typical DC bus voltage waveform after the rectifier.

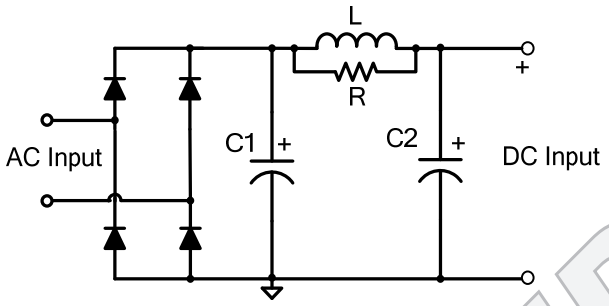


Figure 11: Input Filter

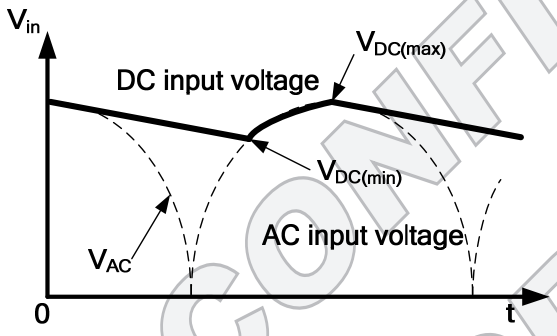


Figure 12: DC Input Voltage Waveform

The bulk capacitors (C1 and C2) filter the rectified AC input. The inductor (L) forms a pi (π) filter with C1 and C2 to restrain the differential mode EMI noise. The resistor (R) in parallel with L restrains the mid-frequency band EMI noise. Normally, R is 1kΩ to 10kΩ.

Usually C1 and C2 are set at 2μF/W to 3μF/W for a universal input condition. For 230V_{AC} single-range applications, cut the capacitor values in half.

A low DC input voltage causes insufficient output current due to the maximum on-duty limitation of the secondary side. To avoid this situation, calculate the minimum input DC voltage with Equation (10):

$$V_{DC(min)} \geq \frac{N_p}{N_s}(V_O + V_D)\frac{D_{S-Max}}{1-D_{S-Max}} \quad (10)$$

If $V_{DC(min)}$ cannot satisfy this expression, use larger input capacitors to increase $V_{DC(min)}$.

Output Capacitor

Low or very low ESR output capacitors are recommended to meet the output voltage ripple requirements. Low ESR capacitors improve the output voltage regulation accuracy at high or low temperatures. Output capacitors with an ESR of tens of mΩ provide better efficiency than high ESR output capacitors.

Output Diode or Synchronous Rectifier

Schottky diodes are recommended for their fast switching speeds and low forward-voltage drops for better high or low temperature CV regulation and efficiency.

If lower average efficiency (3% to 4%) is acceptable, replace the output diode with a fast or ultra-fast diode to reduce cost. Re-adjust the resistor divider values for an accurate output voltage since the forward voltage drop is higher than the Schottky diode.

If the circuit has a high efficiency requirement, it is recommended to use a synchronous rectifier (SR) instead. The MP6906 is a suitable SR controller where the output voltage is low and there is no need for a secondary auxiliary winding. Figure 13 shows a typical SR circuit. The MP6906 is available in a SOT23-6 package, which does not require extra PCB dimensions or external components.

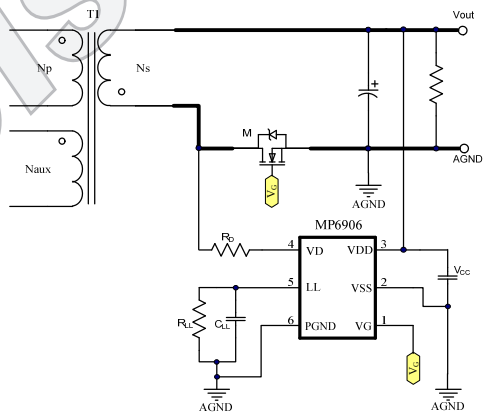


Figure 13: Synchronous Rectifier

Leakage Inductance

The transformer's leakage inductance decreases system efficiency and affects either the output current or voltage constant precision. The transformer structure can be optimized to minimize the leakage inductance. The leakage inductance should be less than 5% of the primary inductance.

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RCD Snubber

The transfomer's leakage inductance causes MOSFET drain voltage spikes and excessive ringing on the drain voltage waveform, which affects the output voltage sampling after the primary MOSFET turns off.

The RCD snubber circuit limits the drain voltage spike. Figure 14 shows the RCD snubber circuit.

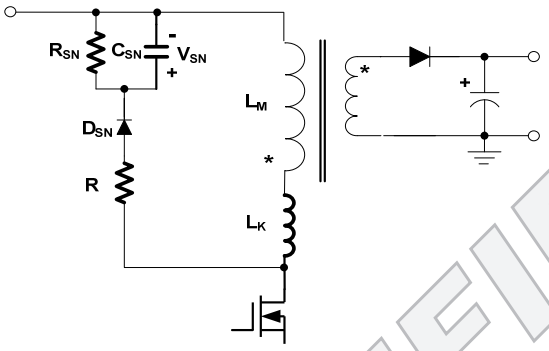


Figure 14: RCD Snubber

Select R_{SN} and C_{SN} to meet the voltage spike requirements and improve system operation.

The power dissipated in the snubber circuit can be approximated with Equation (11):

$$P_{SN} = \frac{1}{2} L_K I_{PK}^2 \frac{V_{SN}}{V_{SN} - N_{PS} V_O} f_S \quad (11)$$

Where L_K is the leakage inductance, V_{SN} is the clamp voltage, and N_{PS} is the turn ratio of the primary-to-secondary side.

Since R_{SN} consumes the majority of the power, calculate R_{SN} with Equation (12):

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}} \quad (12)$$

The maximum ripple of the snubber capacitor voltage is then calculated with Equation (13):

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} R_{SN} f_S} \quad (13)$$

Generally, a 15% ripple is reasonable. The previous equation can also be used to estimate C_{SN}.

Select a time constant ($t = R_{SN} x C_{SN}$) less than 0.1ms for better CV sampling.

The RCD resistor is a trade-off based on the power loss and the acceptable clamp voltage in practical applications.

The damping resistor in series with the RCD has a relatively large value to prevent any excessive voltage ringing that can affect the CV sampling and increase the output ripple. Use a damping resistor value in the range of 100Ω to 500Ω to restrain the drain voltage ringing.

Divided Resistor

For better application performance, select the resistor divider values from 10kΩ to 100kΩ to limit noise from adjacent components on FB. An RC filter can be inserted between the resistor divider and FB to sense purified voltage. The C_{FB} value is recommended to be several pF, and R_{FB} is recommended to be between 1kΩ and 2kΩ. R_{FB} can also limit substrate injection current effects (see Figure 15).

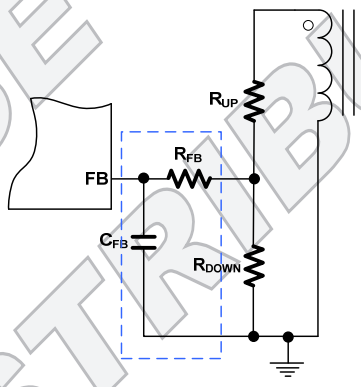


Figure 15: Feedback Resistor Divider Circuit

For accurate CV regulation, the accuracy of these feedback resistors should be at least 1%.

Dummy Load

When the system operates without any load, the output voltage rises above normal operation because of the minimum switching frequency limitation. Use a dummy load for good load regulation. The dummy load is a trade-off between efficiency and load regulation. For example, a large dummy load can deteriorate efficiency and the no-load consumption. For most applications, several mWs for a dummy load is reasonable.

Maximum Switching Frequency

The maximum switching frequency should be limited by the sampling point. Figure 7 and EC table show the relationship of R_{CS} and the sampling point. The secondary on time must be longer than the maximum $T_{FBS-Max}$. Calculate T_{S_ON} with Equation (14):

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$$T_{S_ON} = I_{PK} \frac{N_S \cdot L_M}{N_P \cdot (V_O + V_D)} > t_{FBS_Max} + t_{FB_SD} \quad (14)$$

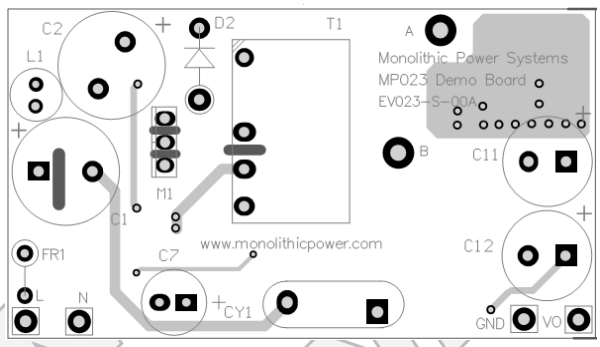
Where $T_{FBS-Max}$ is the FB maximum sampling time, and t_{FB_SD} is the FB sampling duration.

Combine Equation (14) and the relationship of R_{CP} and D_{S-Max} shown in Table 1 to fix the maximum switching frequency.

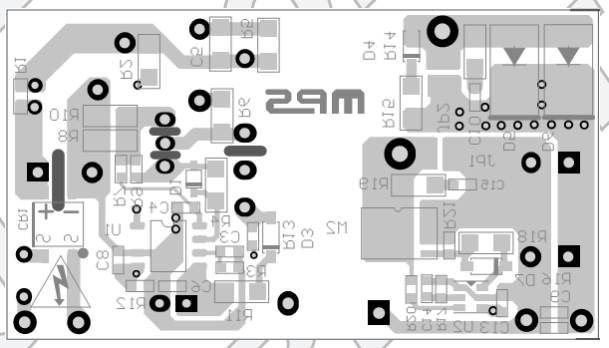
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, good EMI, and good thermal performance. For best results, refer to Figure 16 and follow the guidelines below.

1. Minimize the loop area formed by the input capacitor, the primary transformer winding, the MOSFET drain source, and the sensing resistor to reduce EMI noise.
2. Minimize the voltage jumping area, such as the MOSFET drain, the anode of the secondary diode, etc. for better EMI.
3. Minimize the clamp circuit loop to reduce EMI.
4. Minimize the secondary loop area of the output diode and output filter to reduce EMI noise. Sufficient copper areas should be provided at the cathode terminal of the output diode to act as a heat sink.
5. Place the AC input away from the switching nodes to minimize any noise coupling that may bypass the input filter.
6. Place the bypass capacitor as close to the IC as possible.
7. Place the feedback resistors next to FB and minimize the feedback sampling loop to minimize noise coupling.
8. Use a single-point connection at the negative terminal of the input filter capacitor for the IC GND and bias winding return.



Top Layer



Bottom Layer

Figure 16: Recommended Layout

Design Example

Table 3 is a design example following the application guidelines.

Table 3: Design Example

V_{IN}	85Vac~265Vac 47Hz/63Hz
V_{OUT}	5V
I_{OUT}	2.4A
f_S	70kHz

Figure 17 shows the detailed application schematic. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUIT

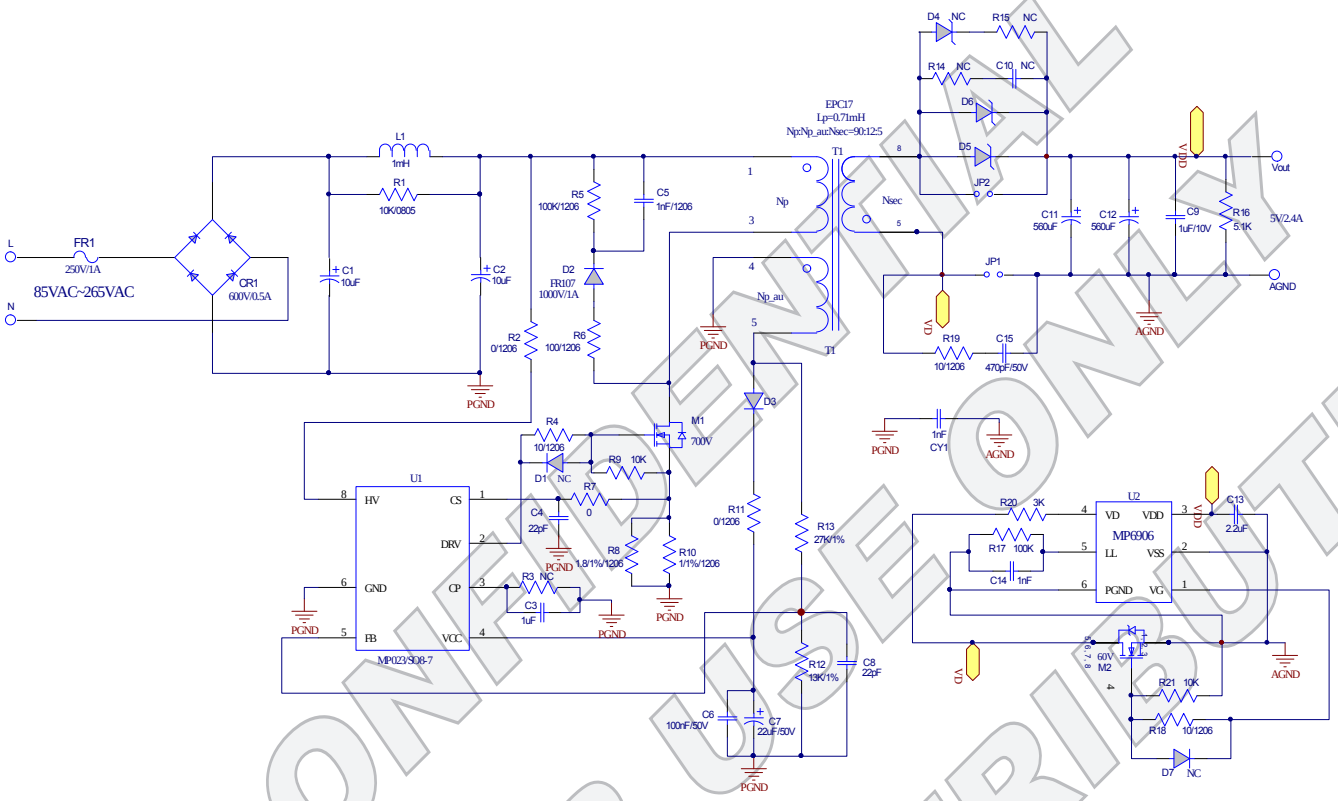
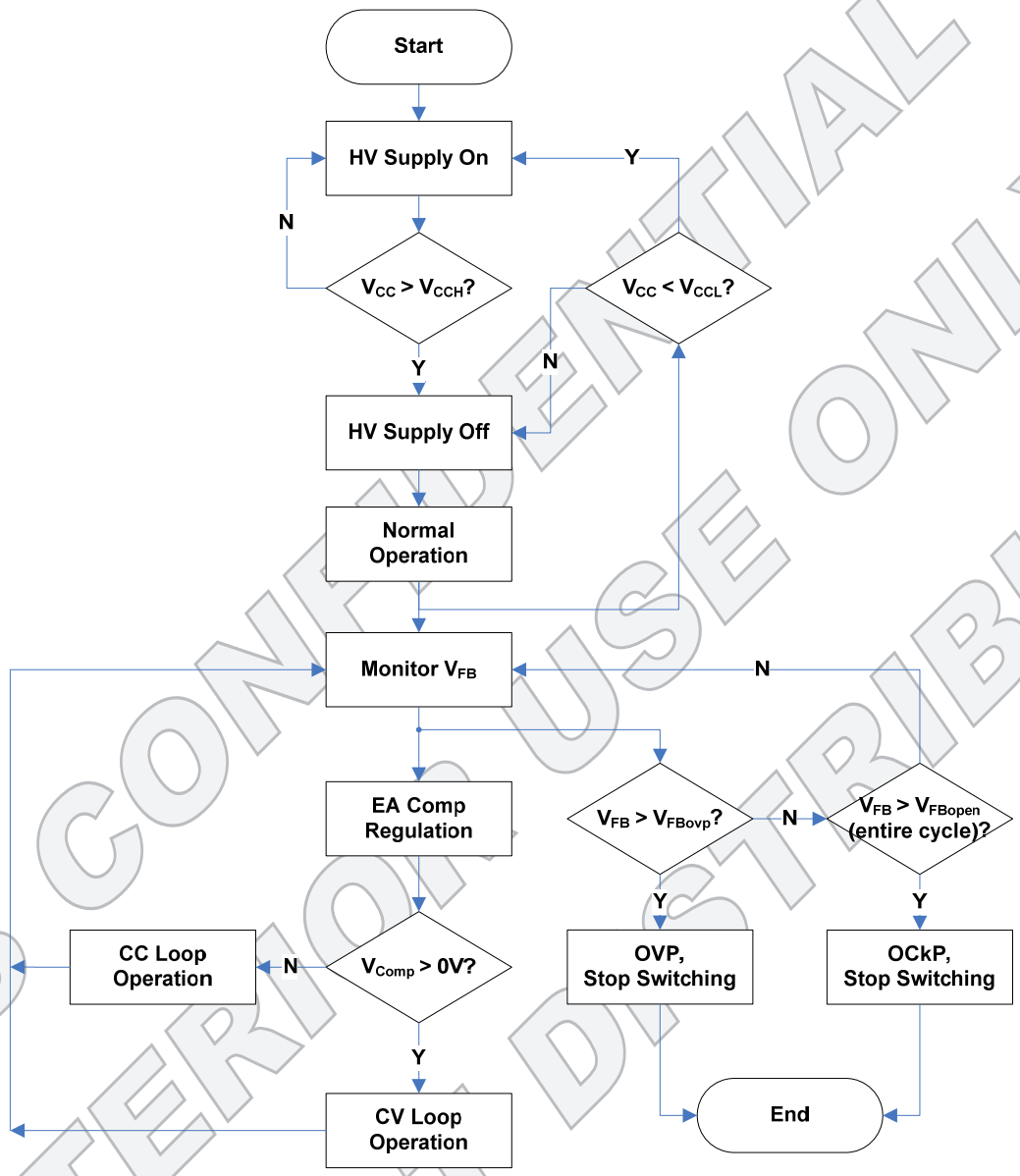


Figure 17: Typical Application—Universal Input, 5V/2.4A Output

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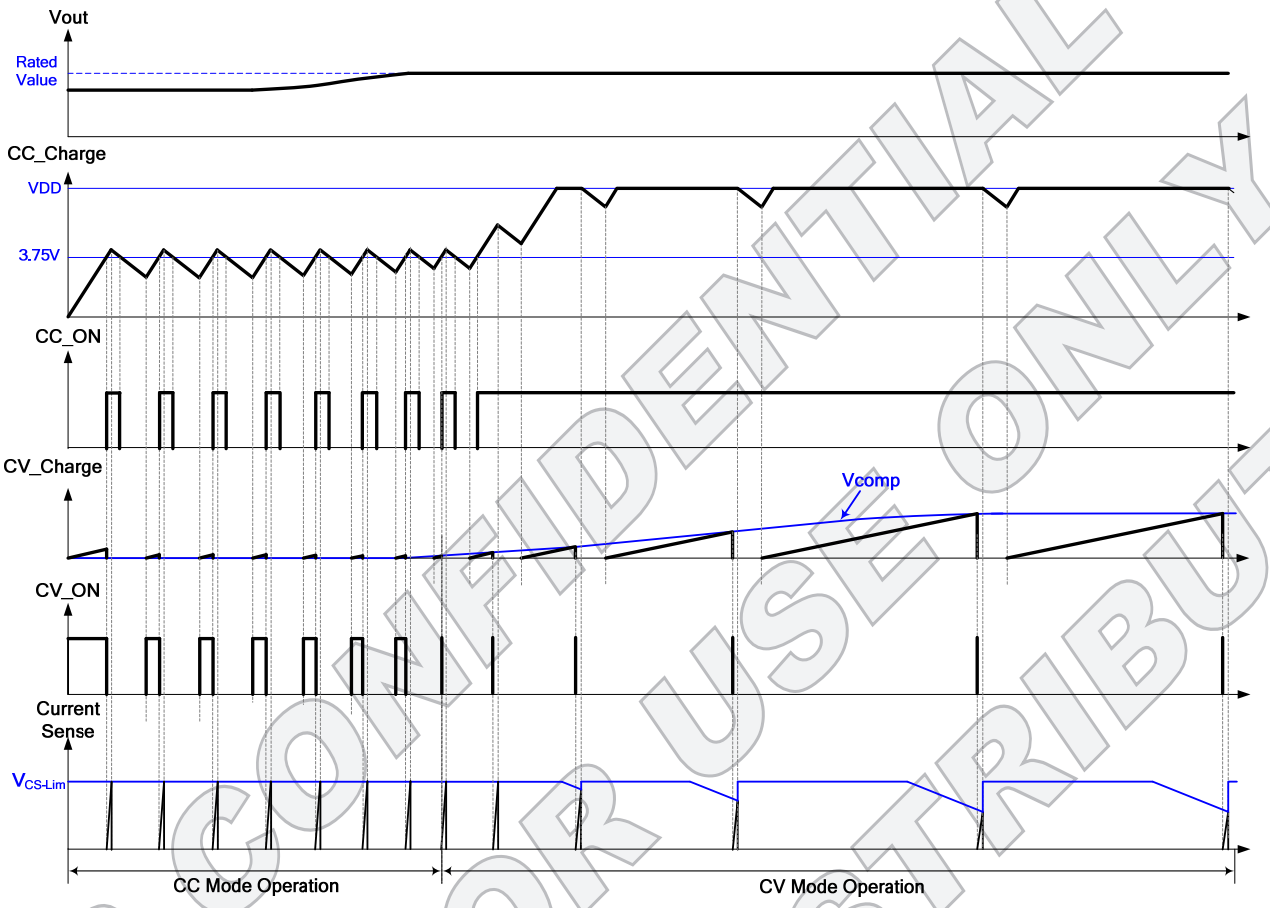
FLOW CHART

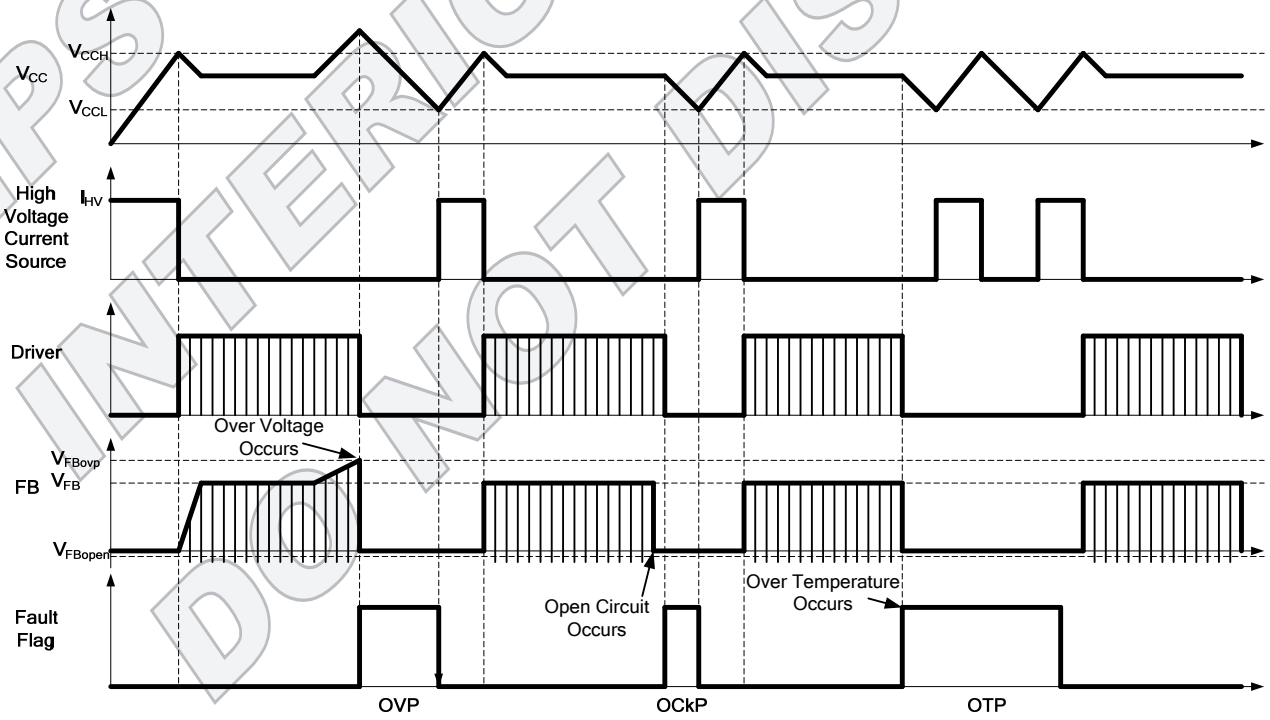


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SIGNAL TIMING SEQUENCE WAVEFORMS



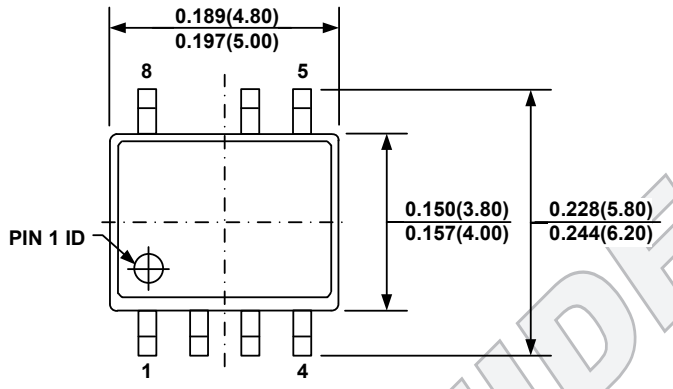


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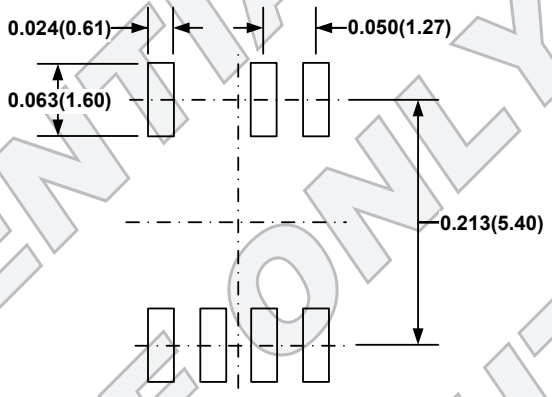
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PACKAGE INFORMATION

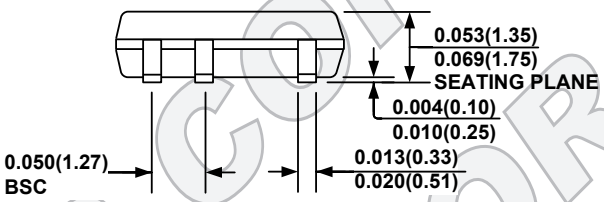
SOIC8-7A



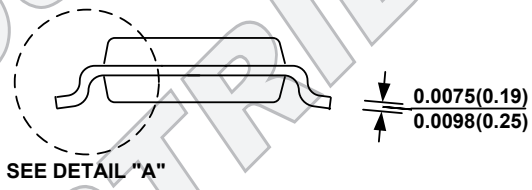
TOP VIEW



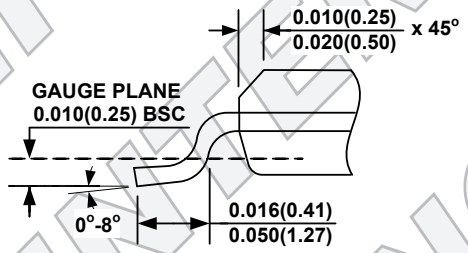
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.

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